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| 31 | US 6031981 A | 20000229 | 10 | Reconfigurable gate array cells for automatic engineering change order | 716/10 |
| 32 | US 5963454 A | 19991005 | 19 | Method and apparatus for efficiently implementing complex function blocks in integrated circuit designs | 716/18 |
| 33 | US 5949692 A | 19990907 | 45 | Hierarchical scan architecture for design for test applications | 716/18 |
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| 36 | US 5831868 A | 19981103 | 35 | Test ready compiler for design for test synthesis | 716/18 |
| 37 | US 5828579 A | 19981027 | 46 | Scan segment processing within hierarchical scan architecture for design for test applications | 716/2 |
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| 39 | US 5801958 A | 19980901 | 95 | Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including interactive system for hierarchical display of control and dataflow information | 716/18 |
| 40 | US 5703789 A | 19971230 | 36 | Test ready compiler for design for test synthesis | 716/4 |
| 41 | US 5696771 A | 19971209 | 46 | Method and apparatus for performing partial unscan and near full scan within design for test applications | 714/726 |
| 42 | US 5663967 A | 19970902 | 12 | Defect isolation using scan-path testing and electron beam probing in multi-level high density asics | 714/737 |
| 43 | US 5598344 A | 19970128 | 51 | Method and system for creating, validating, and scaling structural description of electronic device | 716/18 |
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| 46 | US 5557531 A | 19960917 | 47 | Method and system for creating and validating low level structural description of electronic design from higher level, behavior-oriented description, including estimating power dissipation of physical implementation | 716/1 |
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